



**Research Lab Computational
Technologies and Applications**
University of Vienna, Austria
<http://rlcta.univie.ac.at>



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The Research Lab Computational Technologies and Applications at the Faculty of Computer Science of the University of Vienna, Austria, invites applications for a

Diploma/Master Thesis in Scientific Computing

"Floating-Point Matrix Multiplication on FPGAs".

FPGAs have evolved to powerful computing platforms. Today, multiple double-precision floating point units can be implemented in parallel, rivaling the performance of CPUs. In contrast to CPUs, however, architectures implemented on FPGAs can be custom-tailored to a specific task, thereby outperforming CPUs by an order of magnitude for selected kernels. Matrix multiplication is ubiquitous in scientific computing and its execution time is a key indicator for overall system performance.

You will learn how FPGAs can be used in high-performance computing, how to implement different architectures for matrix multiplication and how to write generic VHDL code. You will extend existing VHDL implementations and learn how to automate Altera Quartus II and to distribute the work load on large servers to synthesize multiple design variants for different FPGAs.

Requirements: VHDL, Experience with Altera QuartusII

Beneficial: basic Linux shell scripting, Tcl, FPGA technology, computer arithmetic

Start: Immediately

Duration: 6 months

Stipend: up to EUR 440,- per month (depending on qualification)

Location: Graz or Vienna.

Contact: DI Bernd Lesser, Bernd.Lesser@univie.ac.at

Literature:

- [1] Y. Dou, S. Vassiliadis, G. K. Kuzmanov, and G. N. Gaydadjiev, "64-bit floating-point FPGA matrix multiplication," in FPGA '05: Proceedings of the 2005 ACM/SIGDA 13th international symposium on Field-programmable gate arrays. New York, NY, USA: ACM, 2005, pp. 86-95. [Online]. Available: <http://dx.doi.org/10.1145/1046192.1046204>